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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,908	ANAND ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *1-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Priority

Acknowledgement is made that no priority either foreign or domestic is claimed for this application and as such the filing date (09/30/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that no Information Disclosure Statement had been provided to the office.

Drawings

The Drawings filed on 8/26/2003 are noted to have been accepted.

Claim Objections

1. Claim 1 is objected to because of the following informalities:

In line 7 of the claim there is no appropriate punctuation

In line 10 there is inappropriate sentence structure.

Appropriate correction is required; the examiner suggests putting a semicolon at the end of line 7 and to put the word "of" between "enables selection" and "a shift chain" in line 10.

2. Claim 14 objected to because of the following informalities:

In line 9, 10 and 12 of the claim there is a different spelling for the "effuse circuit" from claim 12 line 2. Appropriate correction is required.

In lines 4-5 there is improper spacing between "bl" and "ow." Appropriate correction is required.

3. Claim 16 is objected to because of informalities in the preamble, "the system of claim 15," the examiner suggests replacing the preamble with the following, "the device of claim 15, wherein the system further comprises."

4. Claim 17 is objected to because of informalities in the preamble, "the system of claim 16," the examiner suggests replacing the preamble with the following, "the device of claim 16, wherein the system further comprises."

5. Claim 19 is objected to because of informalities in the preamble, "the method of claim 18," the examiner suggests replacing the preamble with the following, "the device of claim 18, with the method further comprising."

Further, claim 19 is objected of the following informalities:

In line 8 of the claim there is a different spelling of "scanIN."

Appropriate correction is required; the examiner suggests replacing "ScanIN" with "scanIN" and for the purposes of this action "ScanIN" will be treated as "scanIN."

6. Claim 20 is objected to because of informalities in the preamble, "the method of claim 19," the examiner suggests replacing the preamble with the following, "the device of claim 19, with the method further comprising."

The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

7. Claims 1-20 are objected to for containing a plurality of elements or steps which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. As per claim 1, it is stated (in lines 4 and 6) a first and second latch, are said to both have a single data input port (line 4 and 6 respectively) and single clock input port (lines 4-5 and 6-7 respectively). It is unclear to the examiner how single input latches (line 2) can have two distinct input ports (input and clock). Appropriate correction or explanation is required for understanding.

Further, claim 1 recites (in lines 8-9 and 10-11) a first clock input and a second clock input at said first and second latches. It is unclear to the examiner how single input latches (line 2) can have two distinct inputs (first and second clock). Appropriate correction or explanation is required for understanding.

Further, claim 1 recites "a scan chain input" and "a shift chain input" (line 12 and 14 respectively). It is unclear to the examiner if these are the same or different from the "scan chain input" and "shift chain input" mentioned previously in lines 8-9 and 10-11 respectively. For the remainder of this action any scan chain inputs and shift chain

inputs will be treated as being the same unless stated to be otherwise. Additionally it is unclear to the examiner how single input latches (line 2) can have two distinct inputs (scan chain and shift chain). Appropriate correction or explanation is required for understanding.

Further, claim 1 recites "input ports of said latches" (line 13), "input ports" (line 14), "multiple inputs" (lines 16-17), and also "single input latches" (line 15). It is unclear to the examiner how single input latches (line 2 and 15) can have input "ports" when they are single input latches. Appropriate correction or explanation is required for understanding.

In view of the 35 USC 112 rejections described above as per claim 1 for purposes of examination the single input latches will be assumed to be a multiplexer.

10. As per claim 3, it is unclear to the examiner how "a data signal" (line 2) is received at "a port" (line 2) of the said latches (line 3) when there is only a single input to these latches (claim 1 line 2). These latches already as described above exceed with a first clock input (claim 1 line 8), a second clock input (claim 1 line 10), a scan chain input (lines 8-9), and shift chain input (lines 10-11) the use of this single input. Appropriate correction or explanation is required for understanding.

Further, claim 3 recites "a data signal" (line 2) is one of "a scan chain input and a shift chain input" (lines 3-4). It is unclear to the examiner if this "data signal" is an additional new scan chain input and shift chain input to said latches different from the scan chain input and shift chain input mentioned in claim 1. For the purposes if examination any and all scan chain inputs and shift chain inputs will be treated as being

the same or different from the "shift chain input" and "scan chain input" in lines Appropriate correction or explanation is required for understanding.

Further, claim 3 recites "a first clock signal" (line 7) and "a second, different clock signal" (line 10). It is unclear to the examiner if these are the same or different from the "first clock input" and "second clock input" mentioned previously in claim 1 lines 8 and 10 respectively. Appropriate correction or explanation is required for understanding. For the remainder of this action any "first clock signal" and "second (, different) clock signal" will be treated as being any input, same or different from the "fist clock input" and "second clock input" of claim 1 lines 8 and 10 respectively.

Further, claim 3 recites the limitation "said single input, scan only latches" in line 13. There is insufficient antecedent basis for these limitations in the claim.

11. As per claims 4-6 all recite the limitation "the system" in line 1. There is insufficient antecedent basis for this limitation in each claim.

Further, claim 4 recites "first and second NAND gates process inputs at substantially the same times" (lines 9-11). It is unclear to the examiner how these two NAND gates can perform a process of inputs at substantially the same time without a delay unit when as stated in claim 3 line 11, only one clock signal is on at a time and each clock signal is an input to one of the NAND gates. Appropriate correction or explanation is required for understanding.

12. As per claim 5, it is stated until a respective clock input shuts off, a delay takes place as to when the two-tiered NAND result is sent to the latches. It is unclear to the examiner when this delayed would takes place when as stated in claim 3, "only one

clock signal is on at a time", indicating to the examiner that a respective clock input (first or second clock) is always off when the other is on. Appropriate correction or explanation is required for understanding.

Further, claim 5 recites, "sending said two-tired NAND result to said latches" in lines 3-4. It is unclear to the examiner if this two-tired NAND result is a new additional input to the single input latches of claim 1 line 2 in the input circuit or the only input to the single input latches, negating the first clock input, scan chain input, second clock input, and shift chain input disclosed in claim 1 lines 8-11 inputted into the latches. Appropriate correction or explanation is required for understanding.

13. As per claim 7, the claim recites the limitation "said OR signal" in line 4. There is insufficient antecedent basis for this limitation in the claim. For the remainder of this action every "OR signal" will be treated as bring the resultant of the "OR gate" of lines 1-2 of the claim.

Further, claim 7 stated that said "OR signal" is utilized as the clock input of said latches in lines 4-5. It is unclear to the examiner if this OR signal is a new additional clock input or the only input clock signal to the single input latches, negating the first clock input and second clock inputs disclosed in claim 1 lines 8-11, or is one of the clock inputs inputted into the single input latches of claim 1 line 2. Appropriate correction or explanation is required for understanding.

Further claim 7 recites the limitations "said first clock signal" and "said second clock signal" in lines 2 and 3 respectively. There is insufficient antecedent basis for this

limitation in the claim. For purposes of examination the "first clock signal" and "second clock signal" will me treated as any input signal.

14. As per claim 8, it should be noted that signals not operations are propagated through devices. The claim states respective operations to be propagated through the device in lines 6-7. Appropriate correction or explanation is required for understanding.

Further claim 8 recites the limitations "said first clock signal" and "said second clock signal" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination the "first clock signal" and "second clock signal" will me treated as any input.

15. As per claim 11, the claim recites the limitation "said semiconductor device" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

16. As per claim 12, it is unclear to the examiner if the "effuse" of line 2 of the claim is the same as the "eFuse" described in the specification (paragraph 0026 and 0014). To help clarify, define "effuse" or show definition in the specification.

Further, claim 12 seems to have a scan only latch select between two different "paths inputted" into a device in lines 5-8. An existing "path" can be selected within a device but cannot be inputted into a device; only data can be inputted into a device. Appropriate correction or explanation is required for understanding.

Further, claim 12 recites the limitation " the scan only latches " and "MUX" in line 9. There is insufficient antecedent basis for these limitations in the claim.

Further, claim 12 recites "passing through said device" either a scan chain "path" or shift chain "path" in lines 10-11. It is unclear to the examiner what is being passed through the device; only data not a "path" can be passed through a device. Appropriate correction or explanation is required for understanding.

Further, claim 12 recites, "serially connected eFuse circuitry" in line 12. It is unclear to the examiner if this "eFuse circuitry" is the same or different from the "effuse circuits" in line 2 of the claim. It is also unclear to the examiner if this "eFuse circuitry" is located within the said circuit within the device or outside said circuit yet within the device. Appropriate correction or explanation is required for understanding. For the purposes of examination in this action it will further be assumed that the "eFuse circuitry" can be either the same or different from the "effuse circuits" and can be either within or just outside the said circuit within the device.

Further, claim 12 recites the limitation " efuse " in line 18. There is insufficient antecedent basis for this limitation in the claim. For the remainder of this office action it will be assumed that "said efuse circuit" in line 18 is the "eFuse circuitry" in line 12.

Further, claim 12 recites the limitation "scan chain path" and "shift chain path" in line 35-36. It is unclear to the examiner what two "paths" the applicant is referring to since it seems that the only paths previously mentioned are paths inputted or passed through the device; as mentioned above only data can pass through or inputted into a device. Appropriate correction or explanation is required for understanding.

17. As per claims 13 and 14 both recite the limitation "the circuit" in line 1. There is insufficient antecedent basis for this limitation in each claim.

18. As per claim 14, it is unclear to the examiner which previous "circuit" is being referring to in line 7 of the claim. Appropriate correction or explanation is required for understanding.

Further, claim 14 seems to claim "only said first and second efuse circuit utilizes processing time for routing said shifted 1 through respective latches" in lines 11-14. It is unclear to the examiner how only the first and second effuse utilizes processing time when a third effuse circuit also as stated in lines 10-11 has a 1 shifted through it's fuse latch, this shifting must take processing time. Appropriate correction or explanation is required for understanding why the shifting time of shifting a 1 through a fuse latch of said third effuse circuit is not included in the processing time

19. As per claim 15, the claim recites the limitation "single input scan only latch" in line 19. There is insufficient antecedent basis for this limitation in the claim.

Further, claim 15 recites, "said resulting output is one of a scan chain input and a shift chain input" in lines 9-10. It is unclear to the examiner how a "single input scan-only latch" as mentioned in line 1 can have two inputs, "scan chain input" and "shift chain input" when it is stated to only have a "single input." Appropriate correction or explanation is required for understanding.

20. As per claims 16 and 17 both recite the limitation "the system" in line 1. There is insufficient antecedent basis for this limitation in each claim.

Further, claim 16 recites a "ScanIN" in line 3 and "shiftIN" in line 7. It is unclear to the examiner what either a "ScanIN" or "shiftIN" is after reading the specification. Appropriate correction or explanation is required for understanding.

Further, the wording of claim 16 indicates that the "NAND result" mentioned in lines 15-16 of the claim is not the same two-tiered NAND gate result of claim 15. The examiner believes that both NAND results were intended to be one in the same and for purposes of this action will be treated as such. Appropriate correction or explanation is required for future understanding.

Further, claim 16 recites "both said first and second NAND gates process their respective inputs at substantially the same time" in lines 9-11. It is unclear to the examiner how both NAND gates can process the inputs at substantially the "same time" when it is indicated in claim 15 line 17 "only one clock signal is on at a time" indicating that there would be a delay in processing. Appropriate correction or explanation is required for future understanding.

21. As per claims 17 and 20, it is stated that until a respective clock input shuts off, a delay takes place as to when the two-tiered NAND result is sent to the latch. It is unclear to the examiner when this delayed would takes place when as stated in claim 15 and 18 respectively, "only one clock signal is on at a time", indicating to the examiner that a respective clock input (first or second clock) is always off when the other is on. Appropriate correction or explanation is required for understanding.

22. As per claim 18, the claim recites "selecting one of a scan chain input and a shift chain input" in lines 9-10. It is unclear to the examiner how the "single input scan only latch" can select from two inputs (scan chain input and shift chain input). Appropriate correction or explanation is required for understanding.

23. As per claim 19, the claim recites a "scanIN" in line 2 and "shiftIN" in line 4. It is unclear to the examiner what either a "scanIN" or "shiftIN" is after reading the specification.

Further, claim 19 recites NANDing a "first clock signal" in line 2. It is unclear to the examiner if this "first clock signal" is the same or different from the "first clock input" of claim 18 line 13 which claim 19 is dependent on. Appropriate correction or explanation is required for understanding.

Further, claim 19 recites NANDing a "second clock signal" in line 4. It is unclear to the examiner if this "second clock signal" is the same or different from the "second clock input" of claim 18 line 16 which claim 19 is dependent on. Appropriate correction or explanation is required for understanding.

Further, claim 19 does not indicate what operation the NANDing of a second clock signal with a shiftIN input is substantially simultaneously performed with in lines 4-5. Appropriate correction or explanation is required for understanding.

24. Claims 2-10 are dependent on claim 1 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

25. Claims 4-5 are dependent on claim 3 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the dependent claim and may not be further considered on their merits.

26. Claim 5 is dependent on claim 4 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the dependent claim and may not be further considered on its merits.

27. Claim 11 is dependent on claim 9 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the dependent claim and may not be further considered on its merits.

28. Claims 13-14 are dependent on claim 12 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

29. Claims 16-17 are dependent on claim 15 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

30. Claim 17 is dependent on claim 16 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the dependent claim and may not be further considered on its merits.

31. Claim 20 is dependent on claim 19 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the dependent claim and may not be further considered on its merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

32. Claims 1, 2, 3, 8, 9, and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by "Multiplexers and Demultiplexers" (hereafter referred to as Multiplexers).

33. As per claim 1, Multiplexers teaches an input circuit (top two MUXes in the figure on page 7 of 10) for providing separate scan and shift paths (top two figures on page 2 of 10) for a device (bottom MUX in the figure on page 7 of 10) untilizing single input latches (top two MUXes in figure on page 7 of 10, top figures on page 2 of 10), said circuit comprising:

A first latch (top left MUX on page 7 of 10) having a single data input port (0 and 1) and single clock input (C) port and an output port (Z);

A second latch (top right MUX on page 7 of 10) having a single data input port (0 and 1) and a single clock input port (C) and an output port (Z);

A first clock input (C0 as a "0") that enables selection of a scan chain input at said first latch and said second latch (X0 and X2 respectively);

A second clock input (C0 as a "1") that enables selection a shift chain input at said first latch and said second latch (X1 and X3 respectively); and

Wherein a selection of a scan chain input (X0 or X2) for passing to said input ports ("0") of said latches occurs exclusive of selection of a shift chain input (X1 or X3) for passing to said input ports ("1"), and vice versa, and wherein said single input latches (top two MUXes in the figure on page 7 of 10) provide functionality of latches that support multiple inputs.

34. As per claim 2, Multiplexers teaches the input circuit described above further comprising:

Means for receiving said scan chain and said first clock input (drawn connections in the figure on page 7 or 10); and

Means for receiving said shift chain input and said second clock input (drawn connections in the figure on page 7 of 10).

35. As per claim 3, Multiplexers teaches the input circuit described above further comprising:

Means for receiving a data signal (X0, X1, X2, X3) at a port ("0", "1") of said latches (top two MUXes in the figure on page 7 of 10), wherein said data signal is one of a scan chain input (X0, X2) and a shift chain input (X1, X3);

Means for accepting the scan chain input into said latches (drawn connections in the figure on page 7 of 10) to commence a scan chain operation (top right figure on page 2 of 10) within said device (bottom MUX in figure one page 7 of 10) then a first clock signal (C1) is on ("1"); and

Means for accepting the shift chain input into said latches (drawn connections in the figure on page 7 of 10) to commence a shift chain operation (top left figure on page 2 of 10) within said device (bottom MUX in figure one page 7 of 10) when a second (C1), different (C1 not C0) clock signal is on ("1"), wherein only one clock signal is on at a time and both said scan chain operation and shift chain operation are supported by said single input latches (figure on page 7 of 10).

36. As per claim 8, Multiplexers teaches the input circuit as described above as per claim 1, wherein the first clock signal (C0) and second clock signal (C1) each provide a select signal ("0" or "1") for respectively receiving either said scan chain input or said shift chain input into said latches (see figures on pages 2 of 10, and 7 of 10), wherein further, the selected input provides a respective scan chain or shift chain operation to be propagated through the device (bottom MUX in figure on page 7 of 10).

37. As per claim 9, Multiplexers teaches the input circuits as described above as per claim 1, wherein said latches are scan only LSSD latches (see figures).

38. As per claim 10, Multiplexers teaches the input circuit as described above as per claim 1, wherein the device is a semiconductor device and said input circuit (top two MUX in figure 7 of 10) is fabricated on said semiconductor device (see figure on page 7 of 10).

Claim 12 is rejected under 35 U.S.C. 102(a) as being anticipated by Maejima (US 6639848).

39. Claims 12, 15, and 18 are rejected under 35 U.S.C. 102(a) as being anticipated by Maejima (US 6639848).

40. As per claim 12, It is the examiners understanding (see 35 U.S.C. 112, second paragraph rejections) that Maejima teaches an input circuit that enables a scan only latch to be utilized to dynamically select from among a scan chain path and a shift chain path being inputted to said device utilizing a series of input clock signals operating as MUX selects for the scan only latches to select either said scan chain path or said shift chain path for passing through said device; serially connected eFuse circuitry

comprising: AND logic having two inputs and an output; a multiplexer (MUX) having a first input, a second input, a select input, and a MUX output, wherein said output of said AND logic is coupled to said select input of said MUX; wherein, said efuse circuit includes a fuse coupled to a switch that is controlled by signals from a fuse latch, a pattern latch, and a program signal source, said pattern latch being programmed with a fuse blow status indicating whether or not said fuse is to be blown during device testing; and means for connecting components and signals of said eFuse circuit to said MUX and said AND logic, wherein said MUX and said AND logic provide a bypass function that determines when a shifted "1" that is serially passed to each of said effuse circuits should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next effuse circuit without forwarding said shifted 1 to said fuse latch; and coupling means for connecting said input circuit to said serially connected eFuse circuit such that both scan chain path and shift chain path are supported within said device utilizing said scan only latches (see Figures 12, 8 7, 5, 3, 2, 1 and column 2 lines 54-64).

41. As per claim 15, It is the examiners understanding (see 35 U.S.C. 112, second paragraph rejections) that Maejima teaches means for receiving the resulting output at the input port of said latch, wherein said resulting output is one of a scan chain input and a shift chain input; means for accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and means for accepting the shift chain input into said latch to commence a shift chain

operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input scan only latch (see Figures 12, 8 7, 5, 3, 2, 1 and column 2 lines 54-64).

42. As per claim 18, It is the examiners understanding (see 35 U.S.C. 112, second paragraph rejections) that Maejima teaches receiving the resulting output at an input port of said latch, wherein said resulting output is a selected one of a scan chain input and a shift chain input; accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latch (see Figures 12, 8 7, 5, 3, 2, 1 and column 2 lines 54-64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

43. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers as applied to claim 3 above, and further in view of Esposito (US 4066882).

44. As per claim 4, Multiplexers teaches the input circuit described above as per claim 3.

Multiplexers does not specifically teach the means for accepting scan chain and shift chain inputs including first level respective NAND gates with respective first and second clock signal inputs which yield respective scan chain and shift chain NAND outputs respectively which are the inputs of a second level NAND gate that yields a subsequently NANDed two-tiered NAND result.

However in an analogous art, Esposito teaches the two-tiered input NAND input means (see figures 11d(7), 11d(6), 10d(4), 10c(6) and 10b(7)) that would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the means for accepting scan chain and shift chain inputs.

Therefore, one would be motivated to have used Esposito's two tiered input NAND input means since NAND gates and two-tiered NAND gate configurations are standard logic for input means as shown by Esposito.

45. As per claim 5, Esposito teach a non-inverting buffer that temporarily delays the two-tiered NAND result prior to sending the two-tiered NAND result as input, wherein

said NAND result is delayed until a respective clock input shuts off (see figure 11d(6) and column 10 line 1 with figure 11d(7)).

46. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers.

47. As per claim 6, Multiplexers teaches the input circuit described as per claim 1.

Multiplexers does not specifically teach the input circuit wherein the second clock input is ANDed with a shift input to yield a shifted second clock input that is utilized as the second clock input for selection of the shift chain input.

However those of ordinary skill in the art at the time the invention was made would recognize that what Multiplexers does not specifically teach as described above is well known in the art.

Therefore, one would be motivated to shift the second clock input by ANDing it with a shift input when it is desired to delayed an input clock or produce a additional clock input, delayed by a set amount of time in-order to perform additional procedures; AND gates are standard logic that is used to shift signals throughout circuitry.

48. As per claim 7, Multiplexers teaches the input circuit described above as per claim 1.

Multiplexers does not specifically teach the input circuit further comprising an OR gate having inputs of said first clock and a result of an ANDing of said second clock with a shift input, wherein an output of said OR gate is utilized as the clock input of said latches (multiplexers).

However those of ordinary skill in the art at the time the invention was made would recognize that Multiplexers does not specifically teach as described above is well known in the art.

Therefore, one would be motivated to OR the first clock with the shifted second clock signal in-order to produce a faster or slower oscillating clock in-order to perform additional procedures; OR gates are standard logic that is used to produce signals throughout circuitry.

49. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers as applied to claim 9 above, and further in view of Maejima (US 6639848).

50. As per claim 11, Multiplexers teaches the input circuit as described above as per claim 9.

Multiplexer does not specifically teach the input circuit wherein the device is an EFUSE device.

However in an analogous art, Maejima teaches that EFUSE devices need input circuitry (see figures 2, 6, 8, 11, 12, and 14).

Therefore, one would be motivated to combine the teaches of Multiplexers and Maejima in-order to minimize circuitry needed to implement different functions within the EFUSE device.

51. Claims 13, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maejima (US 6639848).

52. As per claims 13, 16, and 19, Maejima substantially teaches the device described above as per claims 12, 15 and 18.

Not disclosed by Maejima is the logic configuration of AND, NAND, and MUX logic elements within the device as the applicant does.

However it would have been obvious to one having ordinary skill in the art at the time the invention was made to have configured AND, NAND, and MUX logic elements within the device as the applicant has so described.

Therefore, one would be motivated to configure AND and MUX logic elements within the device in such a configuration since it is well known in that art to interconnect different logic elements in various different configurations in-order to have the configuration of logic elements perform design specific operations.

53. As per claim 14, Maejima teaches said effuse circuit is a first effuse circuit and is serially connected to at least a second effuse circuit whose fuse bl ow status indicates no blowing of its fuse and a third effuse circuit whose fuse blow status indicates a blowing of its fuse, said circuit comprising: means for routing said shifted 1 through said fuse latch of said first efuse circuit, bypassing a fuse latch of said second efuse circuit and routing said shifted 1 through a fuse latch of said third effuse circuit, wherein only said first efuse circuit and said second efuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches (column 2 lines 54-64).

54. As per claim 17, Maejima teaches a buffer that temporarily delays the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the input, wherein said NAND result is delayed until a respective clock input shuts off (figures 3, 14, and 15).

55. As per claim 20, Maejima teaches buffering the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the inputs, wherein said NAND result is delayed until a respective clock input shuts off (figures 3, 14, and 15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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